APPARATUS AND METHOD FOR M-ARY DEMODULATION IN A DIGITAL COMMUNICATION SYSTEM

ABSTRACT OF THE DISCLOSURE

A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of the orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M = 2^N$. The demodulator comprises: 1) a Logic 0 input detector for comparing each of the M binary bits of the serially received orthogonal modulation codes to a Logic 0 and outputting a +1 signal if a match occurs and outputting a -1 signal if a match does not occur; 2) a summation circuit comprising S accumulators; 3) a Logic 0 switch array comprising S switches, wherein a Kth one of the S switches in the Logic 0 switch array couples an output of the Logic 0 input detector to a first input of a Kth one of the S accumulators; 4) a storage array for storing the S orthogonal modulation codes; and 5) control circuitry for synchronously applying the M bits in a Kth one of the S orthogonal modulation codes in the storage array as a switch control signal to the Kth switch in the Logic 0 switch array so that each Logic 0 binary data in the Kth orthogonal modulation code closes the Kth switch in the Logic 0 switch array, thereby connecting the output signal of the Logic 0 input detector to the

first input of the Kth accumulator.